

FIG.1

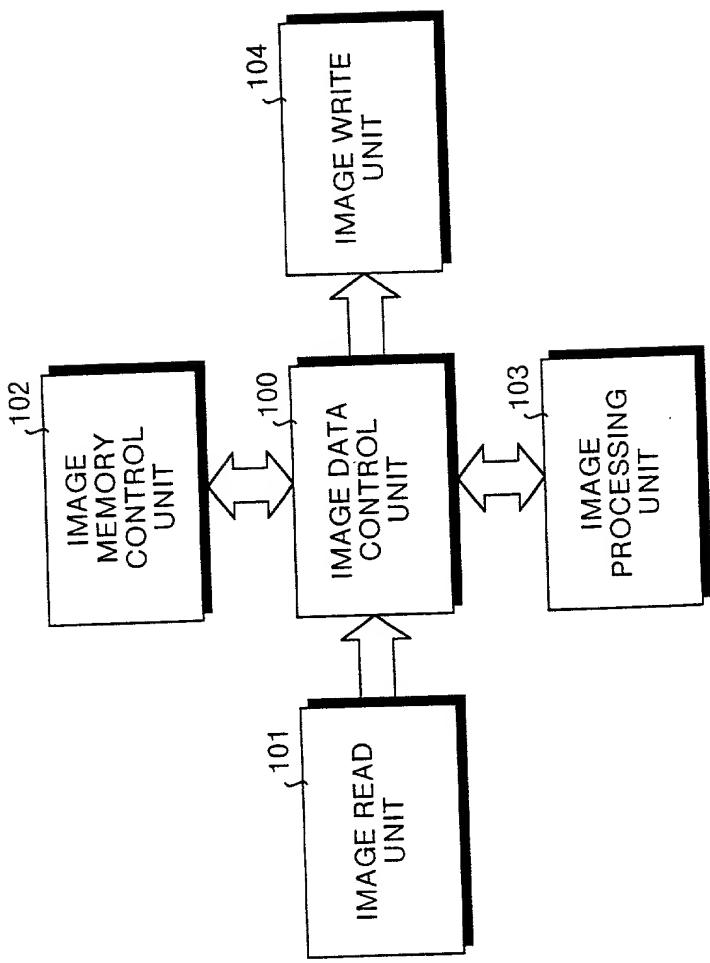


FIG. 2

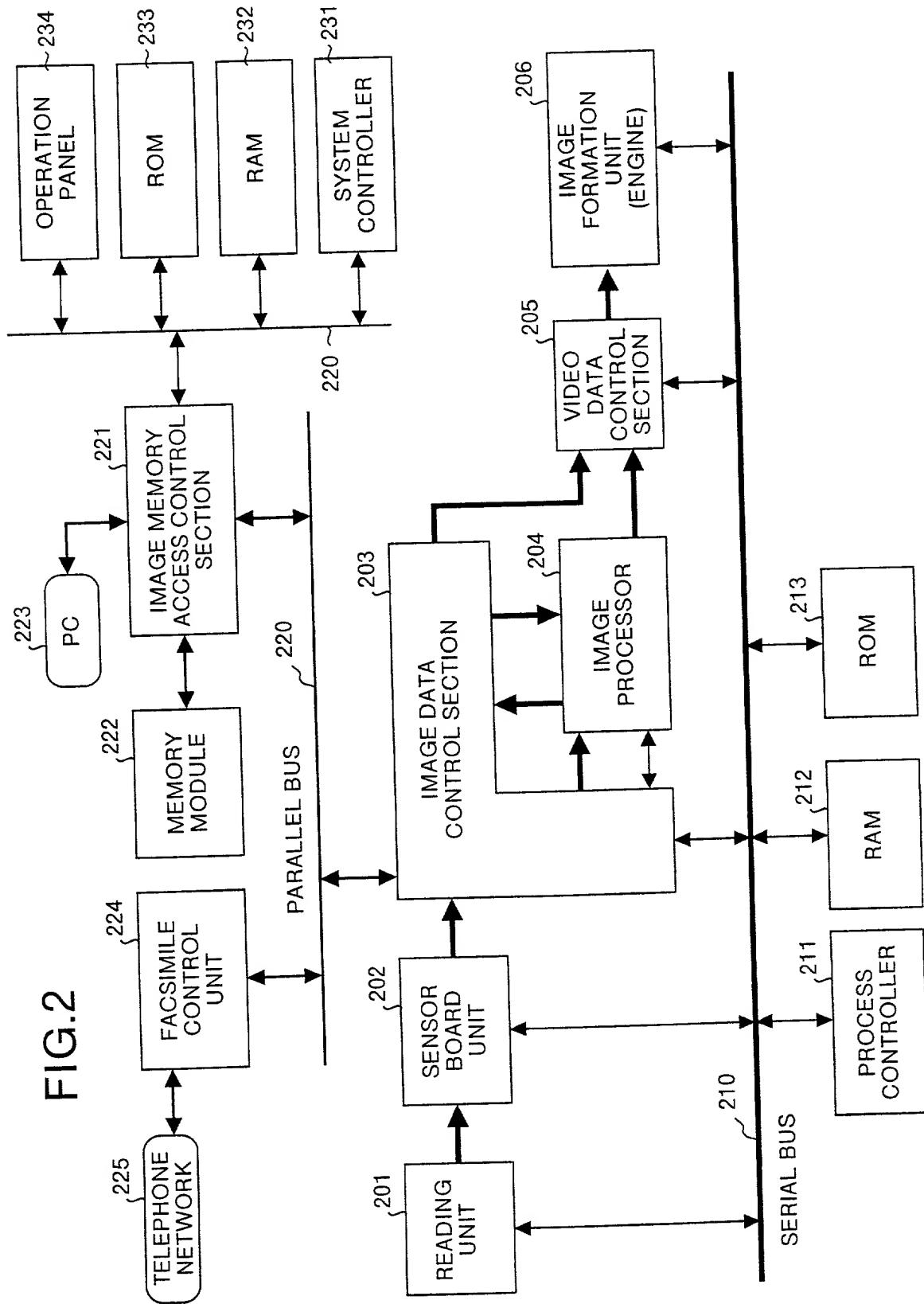


FIG.3

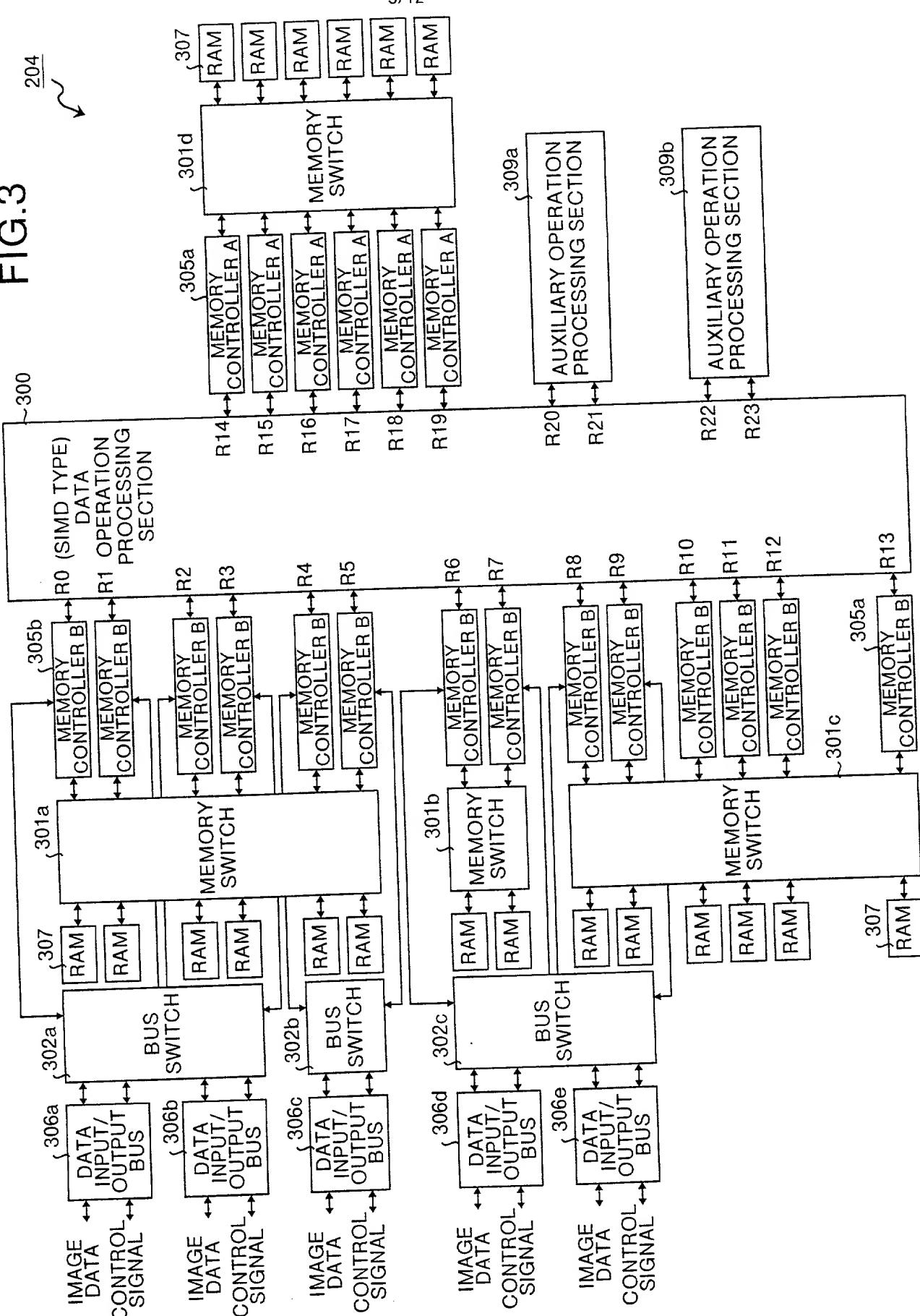


FIG. 4

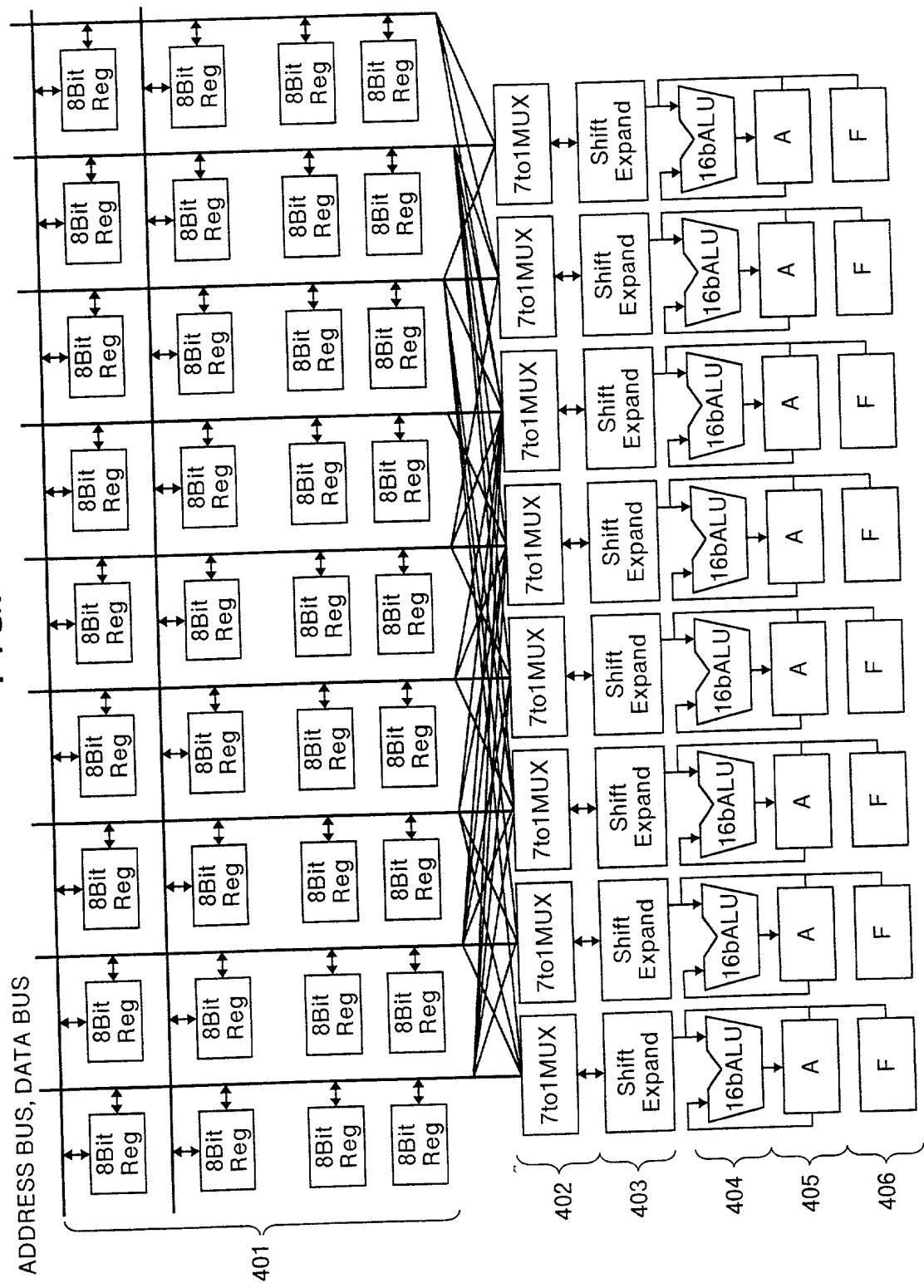


FIG.5

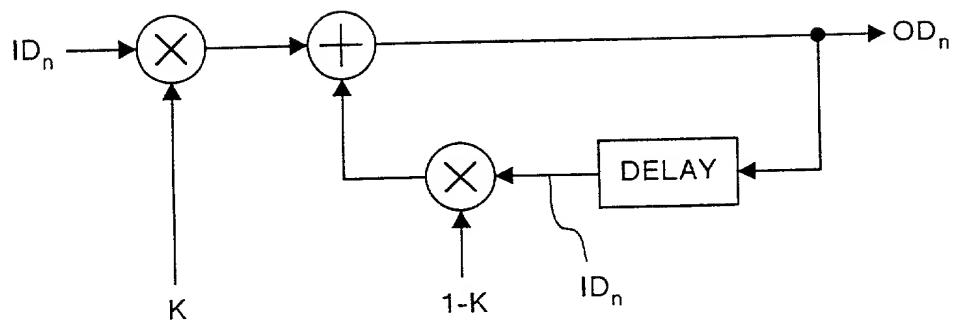


FIG.6

MODE	REGISTER 0 (R0)	REGISTER 1 (R1)	REGISTER 2 (R2)	REGISTER 3 (R3)	REGISTER 4 (R4)	REGISTER 5 (R5)
A	TWO RAMS/TWO RAMS NORMAL/TOGGLE			ONE RAM/TWO RAMS NORMAL/TOGGLE		ONE RAM/TWO RAMS NORMAL/TOGGLE
B	TWO RAMS NORMAL	ONE RAM NORMAL	—	ONE RAM NORMAL	ONE RAM/TWO RAMS NORMAL/TOGGLE	ONE RAM/TWO RAMS NORMAL/TOGGLE
C	TWO RAMS TOGGLE	—	—	—	ONE RAM/TWO RAMS NORMAL/TOGGLE	ONE RAM/TWO RAMS NORMAL/TOGGLE
D	THREE RAMS NORMAL	—		ONE RAM/TWO RAMS NORMAL/TOGGLE	ONE RAM NORMAL	—
E	THREE RAMS NORMAL	ONE RAM NORMAL	—	ONE RAM NORMAL/TOGGLE	ONE RAM NORMAL	—
F	THREE RAMS NORMAL	—		THREE RAMS NORMAL	—	—
G	THREE RAMS TOGGLE	—	—	—	—	—

7/12

FIG.7

REGISTER 0,2,4 (R0,R2,R4)	REGISTER 1,3,5 (R1,R3,R5)
ONE RAM NORMAL	ONE RAM NORMAL
ONE RAM TOGGLE	—
TWO RAMS NORMAL	—

FIG.8

MODE	REGISTER 6 (R6)	REGISTER 7 (R7)
H	ONE RAM NORMAL	ONE RAM NORMAL
I	ONE RAM TOGGLE	—
J	TWO RAMS NORMAL	—

## FIG.9

MODE	INPUT/OUTPUT OF REGISTER 0 (R0)	INPUT/OUTPUT OF REGISTER 1 (R1)	INPUT/OUTPUT OF REGISTER 2 (R2)	INPUT/OUTPUT OF REGISTER 3 (R3)
K	LOWER 8 BITS OF DATA INPUT/OUTPUT BUS 0	UPPER 8 BITS OF DATA INPUT/OUTPUT BUS 0	LOWER 8 BITS OF DATA INPUT/OUTPUT BUS 1	UPPER 8 BITS OF DATA INPUT/OUTPUT BUS 1
L	LOWER 8 BITS OF DATA INPUT/OUTPUT BUS 0	UPPER 8 BITS OF DATA INPUT/OUTPUT BUS 0	16 BITS OF DATA INPUT/OUTPUT BUS 1	—
M	LOWER 8 BITS OF DATA INPUT/OUTPUT BUS 0	UPPER 8 BITS OF DATA INPUT/OUTPUT BUS 0	—	16 BITS OF DATA INPUT/OUTPUT BUS 1
N	16 BITS OF DATA INPUT/OUTPUT BUS 0	—	LOWER 8 BITS OF DATA INPUT/OUTPUT BUS 1	UPPER 8 BITS OF DATA INPUT/OUTPUT BUS 1
O	16 BITS OF DATA INPUT/OUTPUT BUS 0	—	16 BITS OF DATA INPUT/OUTPUT BUS 1	—
P	16 BITS OF DATA INPUT/OUTPUT BUS 0	—	—	16 BITS OF DATA INPUT/OUTPUT BUS 1
Q	—	16 BITS OF DATA INPUT/OUTPUT BUS 0	LOWER 8 BITS OF DATA INPUT/OUTPUT BUS 1	UPPER 8 BITS OF DATA INPUT/OUTPUT BUS 1
R	—	16 BITS OF DATA INPUT/OUTPUT BUS 0	16 BITS OF DATA INPUT/OUTPUT BUS 1	—
S	—	16 BITS OF DATA INPUT/OUTPUT BUS 0	—	16 BITS OF DATA INPUT/OUTPUT BUS 1
T	32 BITS OF DATA INPUT/OUTPUT BUSES 0 AND 1	—	—	—
U	—	32 BITS OF DATA INPUT/OUTPUT BUSES 0 AND 1	—	—

## FIG.10

MODE	INPUT/OUTPUT OF REGISTER 4 (R4)	INPUT/OUTPUT OF REGISTER 5 (R5)
V	LOWER 8 BITS OF DATA INPUT/ OUTPUT BUS 2	UPPER 8 BITS OF DATA INPUT/ OUTPUT BUS 2
W	16 BITS OF DATA INPUT/ OUTPUT BUS 2	—
X	—	16 BITS OF DATA INPUT OUTPUT BUS 2

FIG.11

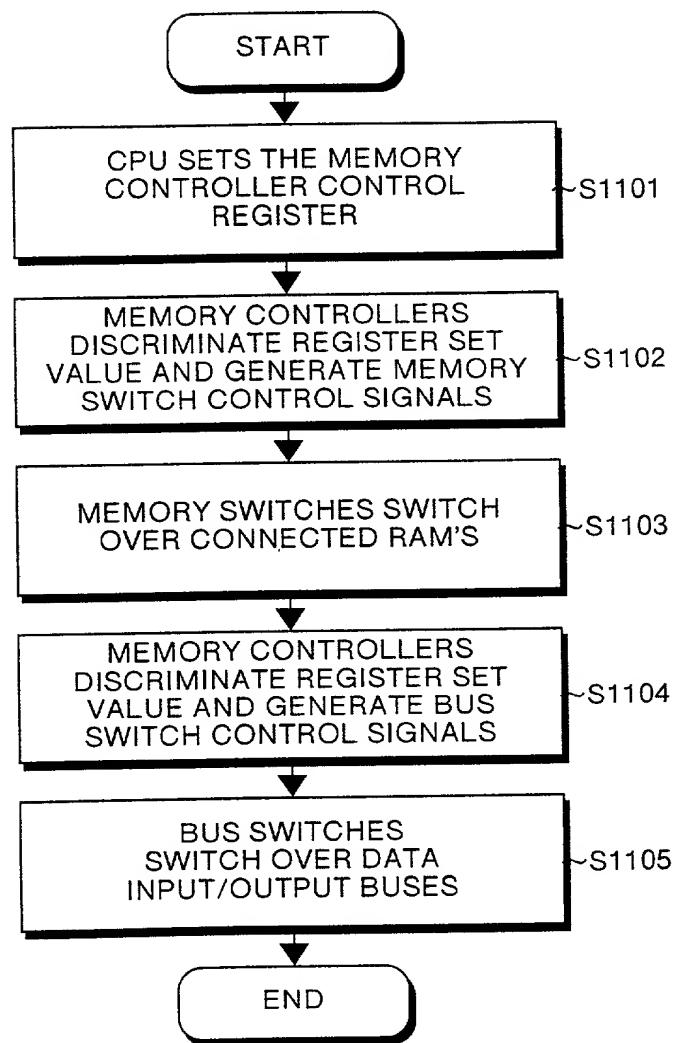


FIG.12

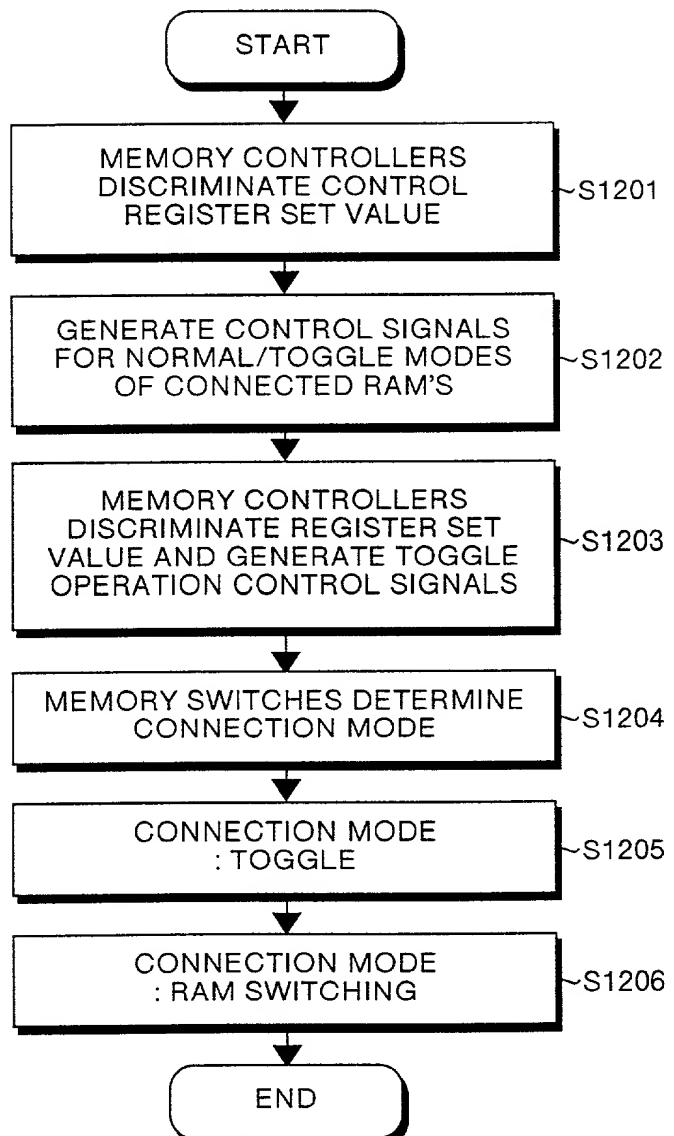


FIG.13

